Notice of Allowability	Application No.	Applicant(s)	
	10/044,242	TAYLOR ET AL.	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the RCE filed on 06/08/05*.

2. ☒ The allowed claim(s) is/are *1-3, 5-24 (renumbered as 1-23)*.

3. ☒ The drawings filed on *10 January 2002* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Examiner's statement for reason for allowance

The following is an examiner's statement for allowance:

1. Claims 1-3 and 5-24 have been allowed.

As per claim 1:

The prior art (Jiang et al. (U.S. PN: 5,748,640)) of record teach or disclose testing of dynamic random access memories (DRAM), and particularly to a built-in self-test (BIST) for a DRAM array incorporated into a microprocessor such that the built-in self-test can operate in mode while functional tests are being run on the microprocessor core (see col. 1, lines 8-12). Jiang et al. in figure 1 teach a system having a built in RAM (volatile memory) (102) and processor (104), and test unit (105) implemented in one or more machines or microcode wherein the test unit is configured to activate the processor and the RAM (see col. 4, lines 19-31). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a volatile memory checker enabled to execute between said periods of activity, said volatile memory checker including test code configured to detect soft errors within said information retained in said volatile memory, said volatile memory being susceptible to soft errors; and said soft errors detected via execution of said volatile memory checker being soft errors occurring during said extended periods of inactivity between said periods of activity of said device; wherein said volatile memory checker includes a timing module enabled to trigger execution of said test mode in response to detection of expiration of a preselected time period and simultaneous detection that said device in a period of inactivity. Consequently, claim 1 is allowed over the prior art.

Claims **1, 3, 5-10,** which is/are directly or indirectly dependent/s of claim 1 are also allowable over the prior art of record.

As per claim 11:

The prior art (Jiang et al. (U.S. PN: 5,748,640)) of record teach or disclose testing of dynamic random access memories (DRAM), and particularly to a built-in self-test (BIST) for a DRAM array incorporated into a microprocessor such that the built-in self-test can operate in mode while functional tests are being run on the microprocessor core (see col. 1, lines 8-12). Jiang et al. in figure 1 teach a system having a built in RAM (volatile memory) (102) and processor (104), and test unit (105) implemented in one or more machines or microcode wherein the test unit is configured to activate the processor and the RAM (see col. 4, lines 19-31). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious performing time based volatile memory checking routines in response to detecting that said device is in said inactive state and a pre-selected time period has elapsed; including checking code space of said volatile memory to detect soft errors within said executable code, said volatile memory being susceptible to said soft errors, wherein said soft errors are those errors occurring within said executable code during said inactive state between said executions of said executable code during said inactive state between said executions of said executable code, said inactive state being a passage of time during which said device is idle; and initiating a selected response upon detecting fatal code error during performing said checking routines. Consequently, claim 11 is allowed over the prior art.

Claims **12-16,** which is/are directly or indirectly dependent/s of claim 11 are also allowable over the prior art of record.

As per claim 17:

The prior art (Jiang et al. (U.S. PN: 5,748,640)) of record teach or disclose testing of dynamic random access memories (DRAM), and particularly to a built-in self-test (BIST) for a DRAM array incorporated into a microprocessor such that the built-in self-test can operate in mode while functional tests are being run on the microprocessor core (see col. 1, lines 8-12). Jiang et al. in figure 1 teach a system having a built in RAM (volatile memory) (102) and processor (104), and test unit (105) implemented in one or more machines or microcode wherein the test unit is configured to activate the processor and the RAM (see col. 4, lines 19-31). Quach (U.S. PN: 6,625,749) teaches an error recovery routine is invoked when the processor detects a soft error while operating in the redundant execution mode (see abstract). Further, Quach teach that an error recovery routine is stored in a memory and the recovery routine is accessed when the processor, implementing a program thread in redundant mode, detects a soft error (see col. 3, lines 53-67 and col. 4, lines 1-8). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious detecting code error in said executable code during storage in said volatile memory, said self-tester being responsive to a time-based test initialization signal for triggering periodic testing said time based test initialization being dependent upon a passage of time intervals related to the time of day and a recovery module responsive to said self-tester to induce an operational sequence that transfers fresh executable code to said input of said volatile memory when said self-tester detects a specific code error condition. Consequently, claim 17 is allowed over the prior art.

Claims **18-21,** which is/are directly or indirectly dependent/s of claim 17 are also allowable over the prior art of record.

As per claim 22:

The prior art (Jiang et al. (U.S. PN: 5,748,640)) of record teach or disclose testing of dynamic random access memories (DRAM), and particularly to a built-in self-test (BIST) for a DRAM array incorporated into a microprocessor such that the built-in self-test can operate in mode while functional tests are being run on the microprocessor core (see col. 1, lines 8-12). Jiang et al. in figure 1 teach a system having a built in RAM (volatile memory) (102) and processor (104), and test unit (105) implemented in one or more machines or microcode wherein the test unit is configured to activate the processor and the RAM (see col. 4, lines 19-31). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious an automated memory checker enabled to execute between said periods of activity, said automated memory checker being configured to execute test code on a timed basis to detect said soft errors within said information stored in said memory, said times bases being dependent upon a passage of time intervals related to a time of day, said soft errors of interest being those errors occurring during said extended periods of inactivity between said periods of activity. Consequently, claim 22 is allowed over the prior art.

Claims **23-24,** which is/are directly or indirectly dependent/s of claim 21 are also allowable over the prior art of record.

Any comment considering necessary by the applicant must be submitted to near than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reason for Allowance".

Conclusion

2. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for after final communications.

Esaw Abraham

Esaw Abraham

Art unit: 2133

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